500.43057X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: H. MATSUSHIGE, et al

Serial No.: 10/649,687

Filed: August 28, 2003

For: STORAGE UNIT AND CIRCUIT FOR SHAPING COMMUNICATION SIGNAL

REQUEST FOR RECONSIDERATION OF PETITION TO MAKE SPECIAL UNDER 37 CFR 1.102(d) and MPEP. §708.02, VIII

MS Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 30, 2004

Sir:

1. Petition

Applicants hereby renews its Petition to make this application **Special** previously submitted on July, 2004, in accordance with 37 CFR §1.102(d) and MPEP 708.02, VIII. The July 22, 2004 Petition was denied by a Decision issued on November 26, 2004 in which the Petitions Examiner stated that the July 22, 2004 Petition failed to recite distinct features of the claimed subject matter. The present Request for Reconsideration of Petition incorporates by reference the July 22, 2004 Petition and provides additional details regarding the claims and how the claimed subject matter is patentable over the references. The present invention is a new application filed in the United States Patent and Trademark Office on August 28, 2003 and as such has not received any examination by the Examiner.

2. Claims

Applicants hereby represent that all the claims in the present application are directed to a single invention. If upon examination it is determined that all the claims presented are not directed to a single invention, Applicants will make an election without traverse as a prerequisite to the granting of special status.

3. Search

Applicants hereby submit that a pre-examination search, a copy of the seach been made by a professional searcher was attached to the July 22, 2004 Petition and therefore is not being resubmitted herewith.

The field of search covered:

Class	Subclasses	Description
318/		**ELECTRICITY: MOTIVE POWER SYSTEMS**
	603	.. Pulse-counting systems
324/		**ELECTRICITY: MEASURING AND TESTING**
	207.25	.. Rotary
360/		**DYNAMIC MAGNETIC INFORMATION STORAGE OR RETRIEVAL**
	51	. Data clocking
	69	AUTOMATIC CONTROL OF A RECORDER MECHANISM
	73.02	... Control of relative speed between carriers
	73.03	... Rotary carrier
710/		**ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT**
	15	. Peripheral monitoring
	58	. Input/Output process timing
711/		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY**
	101	. Specific memory composition
	112	... Direct access storage device (DASD)
	117	. Hierarchical memories
	147	. Shared memory area

167 . Access timing
170 . Memory configuring

The above subclasses represent areas deemed to contain subject matter of interest to one or more of the search features. Please note that relevant references may be classified outside of these areas. The integrity of the search is based on the records as presented to us by the United States Patent and Trademark Office (USPTO). No further integrity studies were performed. Also a key word search was performed on the USPTO full-text database including published U.S. patent applications.

4. Copy of References

A listing of all references found by the professional searcher is provided by a Form PTO-1449 and copies of the references and the Form PTO-1449 are submitted as part of an Information Disclosure Statement (IDS) filed on July 22, 2004. A copy of said July 22, 2004 Information Disclosure Statement without the references is being attached herewith.

5. Detailed Discussion of the References and Distinctions Between the References and the Claims

Below is a discussion of the references uncovered by the search and cited in the IDS filed on even date that appear to be most closely related to the subject matter encompassed by the claims of the present application, and which discussion particularly points out how Applicants' claimed subject matter is distinguishable over those references. All other references uncovered by the search and cited in the IDS filed on July 22, 2004 (a copy of said Information Disclosure Statement is attached) are **not** treated in detail herein.

a. Detailed Discussion of the References

Aikawa et al. (U.S. Patent No. 5,155,638), assigned to Teac Corporation, provides for a Compatible Data Storage Apparatus for Use with Disk Assemblies of Two or More Different Storage Capacities. Discussed is a compatible data storage apparatus having a transducer for writing and reading data on first and second replaceable disk assemblies of different storage capacities at first and second data transfer rates under control of a host system. Two disk sensors may be employed for discriminating between two different types of disks, preferably there may also be included a mode means for inputting from the host system a mode signal indicative of first a first mode in which data is written and read at first and second data transfer rate (see column 1, lines 58-63 and column 2, lines 18-21and 24-28).

Olarig et al. (U.S. Patent No. 6,530,007 B2), assigned to Compaq Information Technologies Group, L.P., provides for a Method and Apparatus for Supporting Heterogeneous Memory in Computer Systems. Discussed is a memory controller capable of supporting heterogeneous memory configurations. The memory controller receives a memory request, identifies a memory and also memory access parameters, and accesses the memory and returns or stores the request. A RAM personality module or memory controller in a second tier is clocked by the same clock received by the first memory controller in the memory system controller (see column 2, lines 41-44 and 47-50, and column 3, lines 2-5).

Piccirillo et al. (U.S. Patent Application Publication No. 2002/0053010 A1) provides for a Method for Supporting Multi-Level Stripping of Non-Homogeneous Memory to Maximize Concurrency. Discussed are host/data controllers **16/18** to be

further coupled to one or more memory controllers. Each of the memory controllers **20A-20E** is further coupled to a segment of main memory (see paragraph 42).

Nagase et al. (U.S. Patent Application Publication No. 2003/0140207 A1), assigned to Hitachi, Ltd., provides for a Hierarchical Storage Apparatus and Control Apparatus Thereof. Disclosed is a storage apparatus including a hierarchical storage unit with a first storage device having a first access speed and a second storage device having a second access speed. Storage controller **201** handles read and write requests to the various storage devices **301**, **302**, **303** and **304** provided in the hierarchical storage area **300**. The controller **201** receives write and read requests from one or more hosts and temporarily stores a corresponding data block in a cache memory **203** (see figure 4, and paragraphs 11 and 33).

b. Distinctions Between the References and the Claims

The present invention as recited in the claims is not taught or suggested by any of the above noted references whether taken individually or in combination with each other or in combination with any of the other references now of record.

The present invention as recited in the claims is directed to a storage unit which includes a channel control portion for receiving a data input/output request, a cache memory for storing data, a disk control portion for performing input/output processing on data in accordance with data input/output request, and a plurality of disk drives for storing data.

According to claims 1 and 2, the storage unit provides that at least two of the disk drives input data to and output data from the disk control portion at different communication speeds. Further, according to the present invention, the storage unit

has a plurality of communication paths provided to connect at least one of the disk drives in such a manner as to constitute a loop defined by the FC-AL fiber channel standards, so that the communication speeds can be set differently for these different communication paths.

According to claims 3-7, the storage unit includes a disk drive for storing data, a disk drive control portion for communicating with the disk drive, a generation portion for generating a clock signal by using a pulse signal transferred for the communication, an identification portion for identifying a frequency of the pulse signal, a frequency division portion for dividing a frequency of a clock signal at a frequency division ratio that corresponds to a frequency of the clock signal and a synchronization portion for synchronizing the pulse signal with the clock signal having the divided frequency.

According to claims 8 and 9, the storage unit is similar to that recited in claim 3 with the exception of providing a communication specification portion for deciding whether the pulse signal satisfies communication specifications when the pulse signal is read in a period of the clock signal, a frequency division portion for dividing a frequency of the clock signal in accordance with a result of the decision and a synchronization portion for synchronizing the pulse signal with the clock signal having the divided frequency.

According to claims 10-12 the present invention provides a circuit for shaping a communication signal having elements similar to that recited in claim 3 with the exception of the elements concerning the storage unit. Thus, according to claims 10-12 the circuit includes the generation portion, the identification portion, the frequency division circuit and the synchronization portion.

According to claim 13 the present invention provides a circuit similar to that recited in claim 8 with the exception of the elements concern the storage unit, namely, the generation portion, the communication specification decision portion, the frequency division portion and the synchronization portion.

The above described features of the present invention, particularly the provision wherein at least two of the disk drives of the storage unit input data to and output data from a disk control portion of the storage unit at different communication speeds, the provision that the storage unit has a plurality of communication paths provided to connect at least one of the disk drives in such a manner as to constitute a loop defined by the FC-AL fiber channel standards, so that the communication speeds can be set differently for these different communication paths, the provision of at least one of a generation portion for generating a clock signal by using a pulse signal transferred for the communication, an identification portion for identifying a frequency of the pulse signal, a frequency division portion for dividing a frequency of the clock signal at a frequency division ratio that correspondence to a frequency of the pulse signal, a synchronization portion for synchronizing the pulse signal with the clock signal having the divided frequency, and a communication specifications decision portion for deciding whether the pulse signal satisfies the communication specification, when the pulse signal is read in a period of the clock signal, are taught or suggested by any of the references of record whether taken individually or in combination with each other.

For example, the above described features of the present invention are not taught to suggested by Aikawa. As per the above, Aikawa teaches a data storage apparatus having a transducer for writing and reading data on first and second

replaceable disk assemblies of different storage capacities at first and second data transfer rate under control of a host system.

The present invention as recited in the claims differs from that taught by Aikawa being that the present invention as recited in the claims provides that at least two of the disk drives of the storage unit input data to and output data from a disk control portion of the storage unit at different communication speeds, that the storage unit has a plurality of communication paths provided to connect at least one of the disk drives in such a manner so as constitute a loop defined by the FC-AL fiber channel standards, so that the communication speeds can be set differently for the different communication paths, and that the storage unit or the circuit for shaping a communication signal includes at least one of a generation portion for generating a clock signal by using a pulse signal transferred for communication, an identification portion for identifying a frequency of the pulse signal, a frequency division circuit for dividing a frequency of the clock signal at a frequency division ratio that corresponds to a frequency of the pulse signal, a synchronization portion for synchronizing the pulse signal with the clock signal having the divided frequency and a communication specifications decision portion for deciding whether the pulse signal satisfies specifications of the communication when the pulse signal is read in a period of the clock signal. These features are clearly not taught or suggested by Aikawa.

The above noted deficiencies of Aikawa are also evident in each of the above described references and each of the other references of record. Therefore, the above described references and the other references of record whether taken individually or in combination with each other still fail to teach or suggest the features of the present invention as recited in the claims.

Based on the above applicants submit that the claims of the present application are patentable over the above described references and the other references of record whether taken individually or in combination with each other.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER & MALUR, P.C., Deposit Account No. 01-2135 (500.43057X00).

Respectfully submitted,

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CIB/jdc
Enclosures